We claim:

1. A method for forming an integrated circuit capacitor, comprising:

forming a dielectric region in a semiconductor substrate;

forming a patterned polysilicon layer on said dielectric region;

forming a dielectric layer over said polysilicon layer;

forming a conductive layer over said dielectric layer;

forming a hardmask layer over said conductive layer;

etching said hardmask layer and partially etching said conductive layer using a dry etch process; and

etching remaining conductive layer using a wet etch process.

2. The method of claim 1 wherein said dry etch process used to etch said hardmask layer and partially etch said conductive

layer is a two step etch process consisting essentially of a first plasma etch step and a second plasma etch step.

3. The method of claim 2 wherein said first plasma etch step is a plasma etch process comprising Cl_2, Ar, and BCl_3.

4. The method of claim 3 wherein said second plasma etch step is a plasma etch process comprising Cl_2, Ar, BCl_3, and N_2.

5. The method of claim 1 wherein said wet etch process is a two step etch process consisting essentially of a first wet etch step and a second wet etch step.

6. The method of claim 5 wherein said first wet etch step comprises spraying a Piranha solution and a SC1 solution.

7. The method of claim 6 wherein said second wet etch step comprises a SC1 megasonic process.

8. A method for forming a high precision integrated circuit capacitor, comprising:

forming a dielectric region in a semiconductor substrate;

forming a patterned polysilicon layer on said dielectric region;

forming a metal silicide on said polysilicon layer;

forming a dielectric layer over said metal silicide layer;

forming a TiN layer over said dielectric layer;

forming a silicon oxide layer over said conductive layer;

etching said silicon layer and partially etching said TiN layer using a two step plasma etch process; and

etching remaining TiN layer using a two step wet etch process.

9. The method of claim 8 wherein said two step etch process consists essentially of a first plasma etch step and a second plasma etch step.

10. The method of claim 9 wherein said first plasma etch step is a plasma etch process comprising Cl_2, Ar, and BCl_3.

11. The method of claim 10 wherein said second plasma etch step is a plasma etch process comprising Cl_2, Ar, BCl_3, and N_2.

12. The method of claim 8 wherein said wet etch process consists essentially of a first wet etch step and a second wet etch step.

13. The method of claim 12 wherein said first wet etch step comprises spraying a Piranha solution and a SC1 solution.

14. The method of claim 13 wherein said second wet etch step comprises a SC1 megasonic process.

15. A method for forming an integrated circuit capacitor in a trench, comprising:

forming a trench in a semiconductor substrate;

forming a first dielectric layer in said trench;

forming a patterned polysilicon layer on said dielectric layer;

forming a metal silicide on said polysilicon layer;

forming a second dielectric layer over said metal silicide layer;

forming a conductive layer over said dielectric layer;

forming a hardmask layer over said conductive layer;

etching said hardmask layer and partially etching said conductive layer using a dry etch process; and

etching remaining conductive layer using a wet etch process.

16. The method of claim 15 wherein said dry etch process used to etch said hardmask layer and partially etch said conductive layer is a two step etch process consisting essentially of a first plasma etch step and a second plasma etch step.

17. The method of claim 16 wherein said first plasma etch step is a plasma etch process comprising Cl_2, Ar, and BCl_3.

18. The method of claim 17 wherein said second plasma etch step is a plasma etch process comprising Cl_2, Ar, BCl_3, and N_2.

19. The method of claim 15 wherein said wet etch process is a two step etch process consisting essentially of a first wet etch step and a second wet etch step.

20. The method of claim 19 wherein said first wet etch step comprises spraying a Piranha solution and a SC1 solution.

21. The method of claim 20 wherein said second wet etch step comprises a SC1 megasonic process.